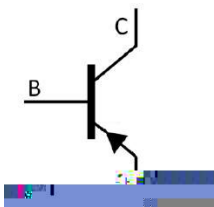


VRW-56 SQS Silicon PNP transistor in a SOT-23 Plastic Package.

Low frequency.

Low frequency power amplifier.



PIN 1 Base PIN 2 Emitter PIN 3 Collector

Parameter	Symbol	Rating	Unit
Collector to Base Voltage	V_{CBO}	-35	V
Collector to Emitter Voltage	V_{CEO}	-30	V
Emitter to Base Voltage	V_{EBO}	-5.0	V
Collector Current	I_C	-500	mA
Collector Power Dissipation	P_C	150	mW
Junction Temperature	T_j	150	
Storage Temperature Range	T_{stg}	-55 150	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector Cut-Off Current	I_{CBO}	$V_{CB}=-35V$ $I_E=0$			-0.1	μA
Emitter Cut-Off Current	I_{EBO}	$V_{EB}=-5.0V$ $I_C=0$			-0.1	μA
DC Current Gain	$h_{FE(1)}$	$V_{CE}=-1.0V$ $I_C=-100mA$	70		240	
	$h_{FE(2)}$	$V_{CE}=-6.0V$ $I_C=-400mA$	25			
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=-100mA$ $I_B=-10mA$		-0.1	-0.25	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=-100mA$ $V_{CE}=-1.0V$		-0.8	-1.0	V
Transition Frequency	f_T	$I_C=-20mA$ $V_{CE}=-6.0V$		200		MHz
Collector Output Capacitance	C_{ob}	$V_{CB}=-6.0V$ $I_E=0$ $f=1.0MHz$				

/ Electrical Characteristic Curve

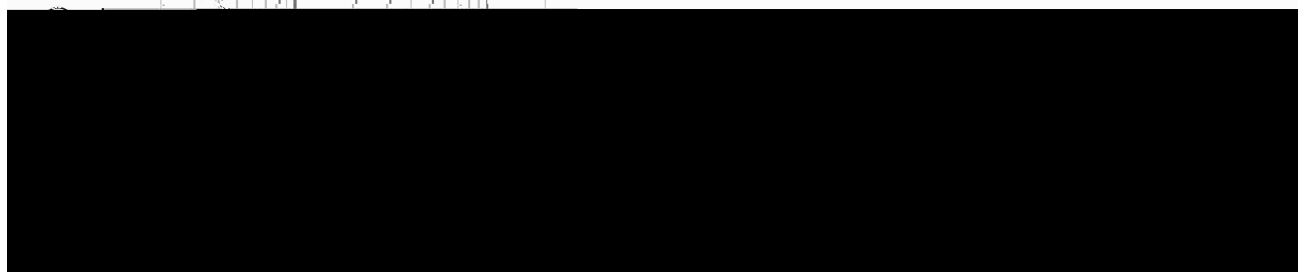
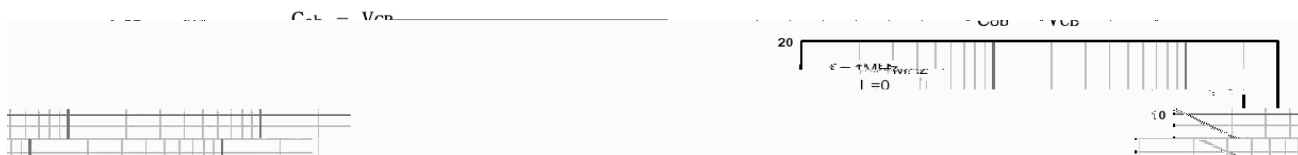
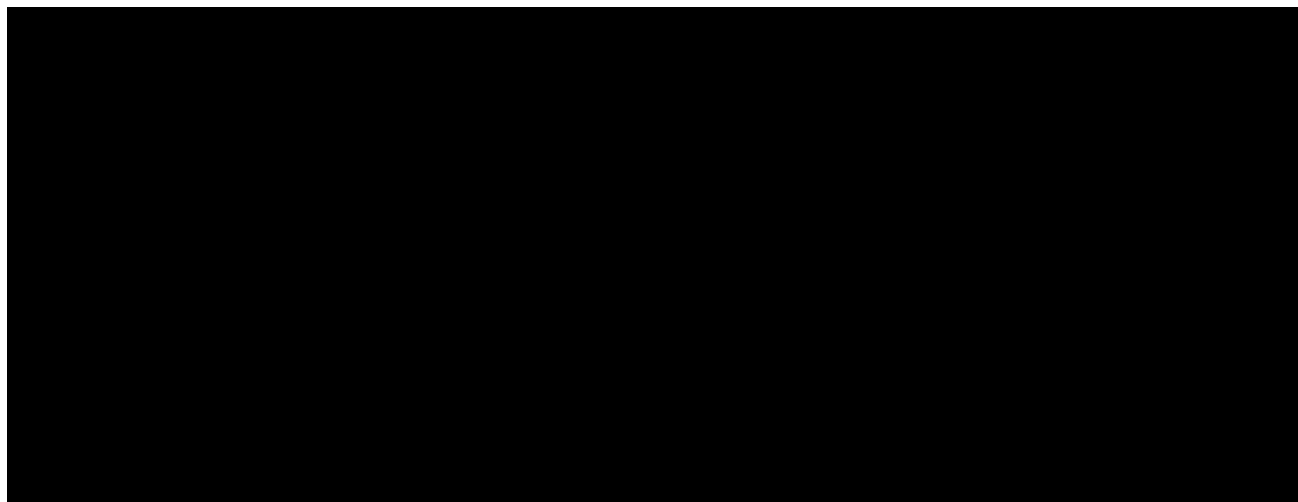
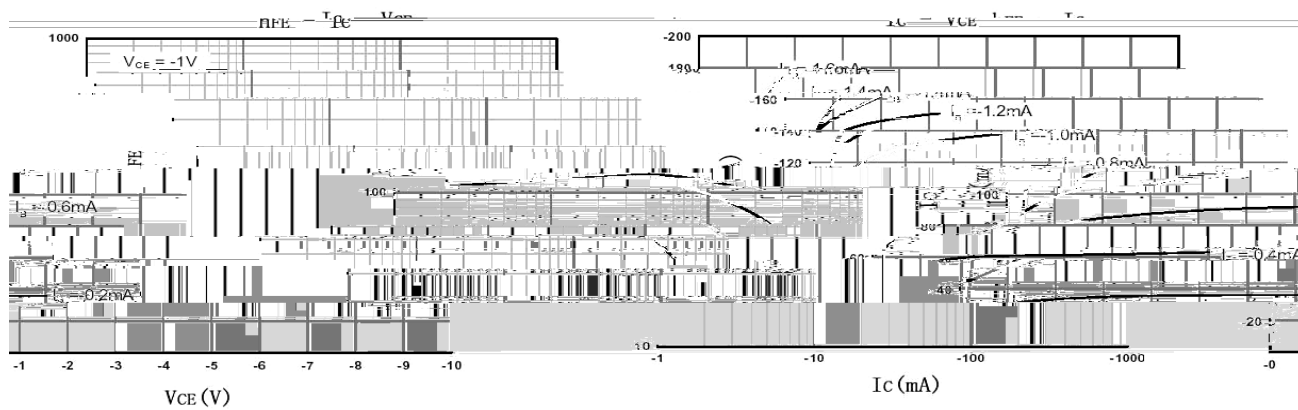
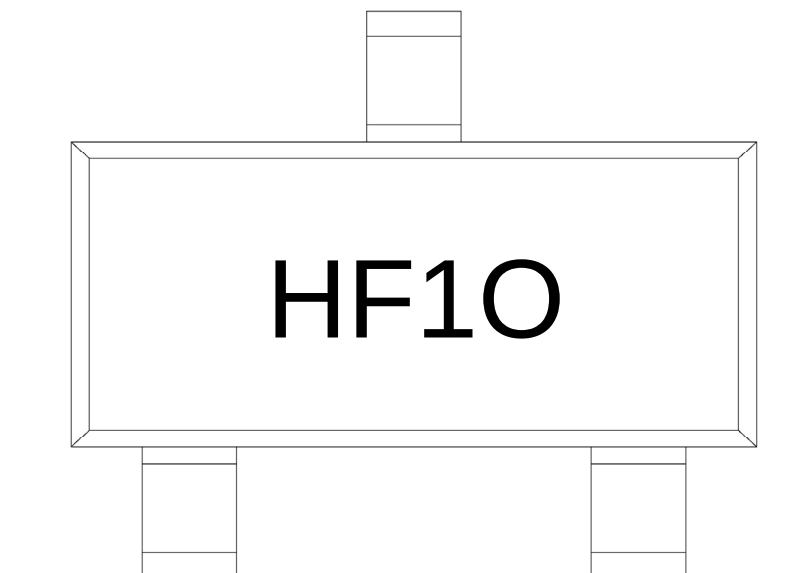


Figure 1: A schematic diagram of a 2D lattice system. The lattice is composed of blue squares representing sites. A central path of sites is highlighted in red, representing the 'red chain'. The lattice is divided into two regions by a vertical dashed line. The left region is labeled 'Left' and the right region is labeled 'Right'. The red chain starts at the left edge and ends at the right edge. The lattice is labeled 'Lattice' at the bottom left and 'Right' at the bottom right.

/ Marking Instructions



H

I4

R h_{IH}

Note:

H Company Code

F1 Product Type Code

O h_{FE} Classifications Symbol Code

() / **Temperature Profile for IR Reflow Soldering(Pb Z**