

Rev.A Sep.-2024

SOP-8 P MOS

P-Channel Enhancement Mode Field Effect Transistor in a SOP-8 Plastic Package.

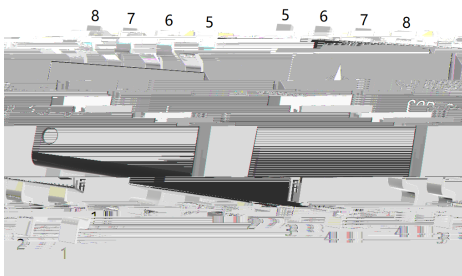
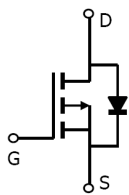
$V_{DS} (V) = -40V$ $I_D = -6.8A$ ($V_{GS} = \pm 20V$)

$R_{DS(ON)}@-10V \leq 35m\Omega$ (Typ. 33m Ω)

$R_{DS(ON)}@-4.5V \leq 60m\Omega$ (Typ. 40m Ω)

HF Product.

Power Management in Notebook computer, Portable Equipment and Battery powered systems.



PIN 1	S	PIN 2	S	PIN 3	S	PIN 4	G
PIN 5	D	PIN 6	D	PIN 7	D	PIN 8	D

See Marking Instructions.

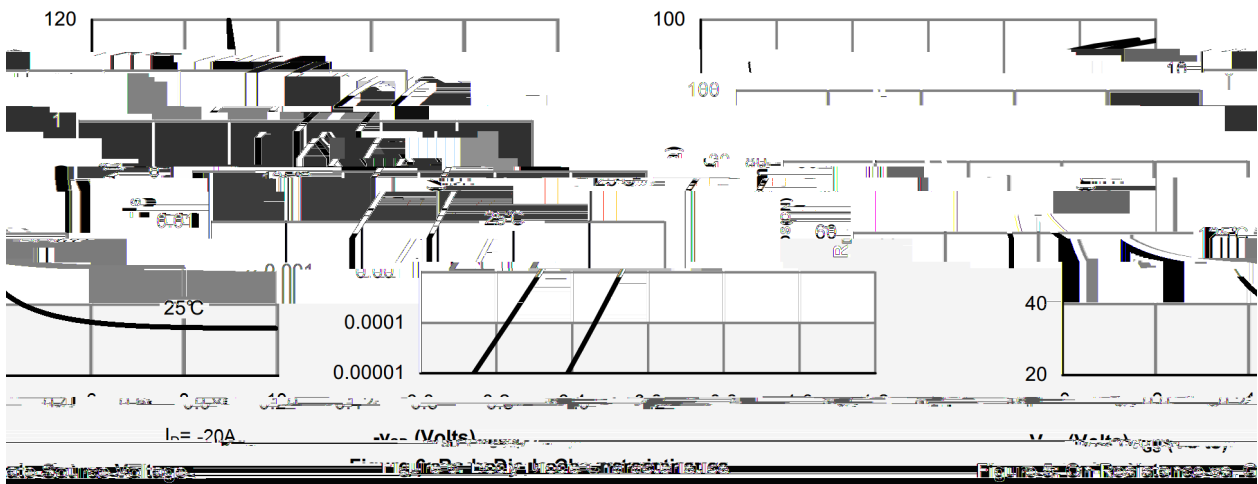
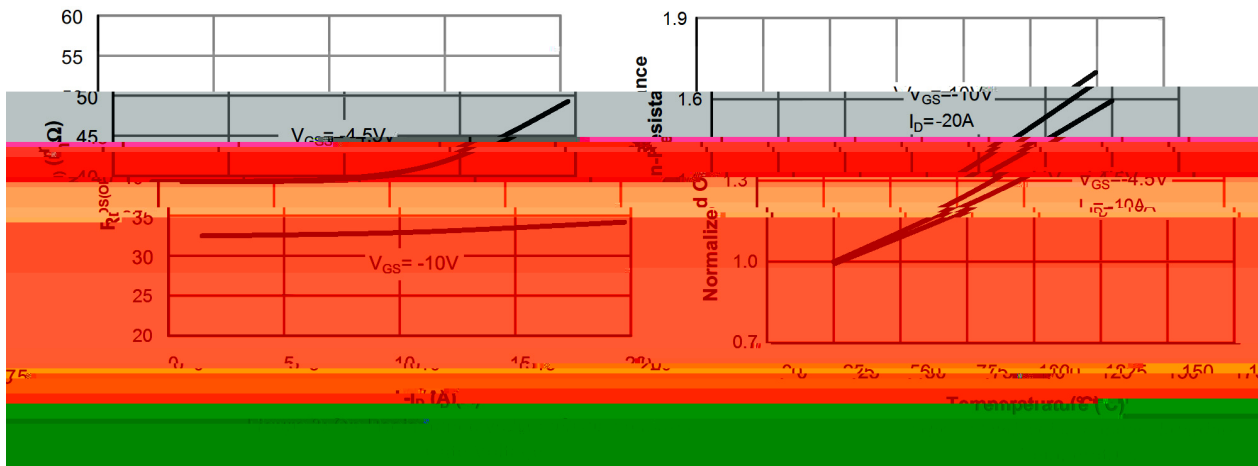
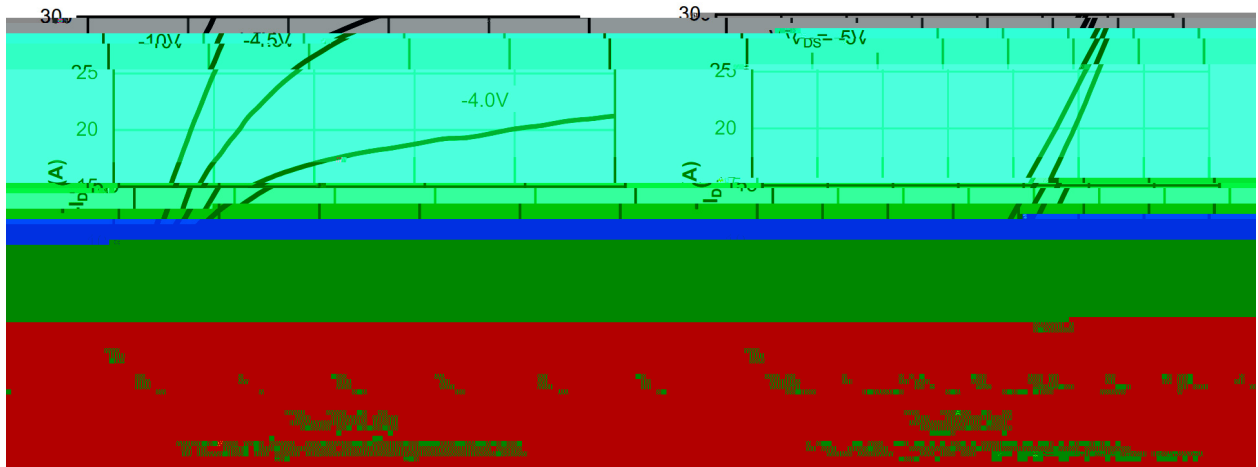
Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-40	V
Drain Current		I_D	-6.8	A
Drain Current - Pulsed		I_{DM}	-30	A
Gate-Source Voltage		V_{GS}	± 20	V
Avalanche Current		I_{AS}	13	A
Single Pulsed Avalanche Energy $L=0.5mH$		E_{AS}	54	mJ
Power Dissipation		P_D	2.7	W
Storage Temperature Range		T_{stg}	-55 150	
Thermal Resistance-Junction to Ambient	$t \leq 10s$	$R_{\theta JA}$	46	/W
	Steady-State		80	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=-250\mu A$	-40	-46		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V$ $V_{GS}=0V$			1.0	μA
Gate-Body Leakage Current Forward	I_{GSS}	$V_{GS}=\pm 20V$ $V_{DS}=0V$			± 0.1	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ $I_D=-250\mu A$	-1.0	-1.4	-2.5	V

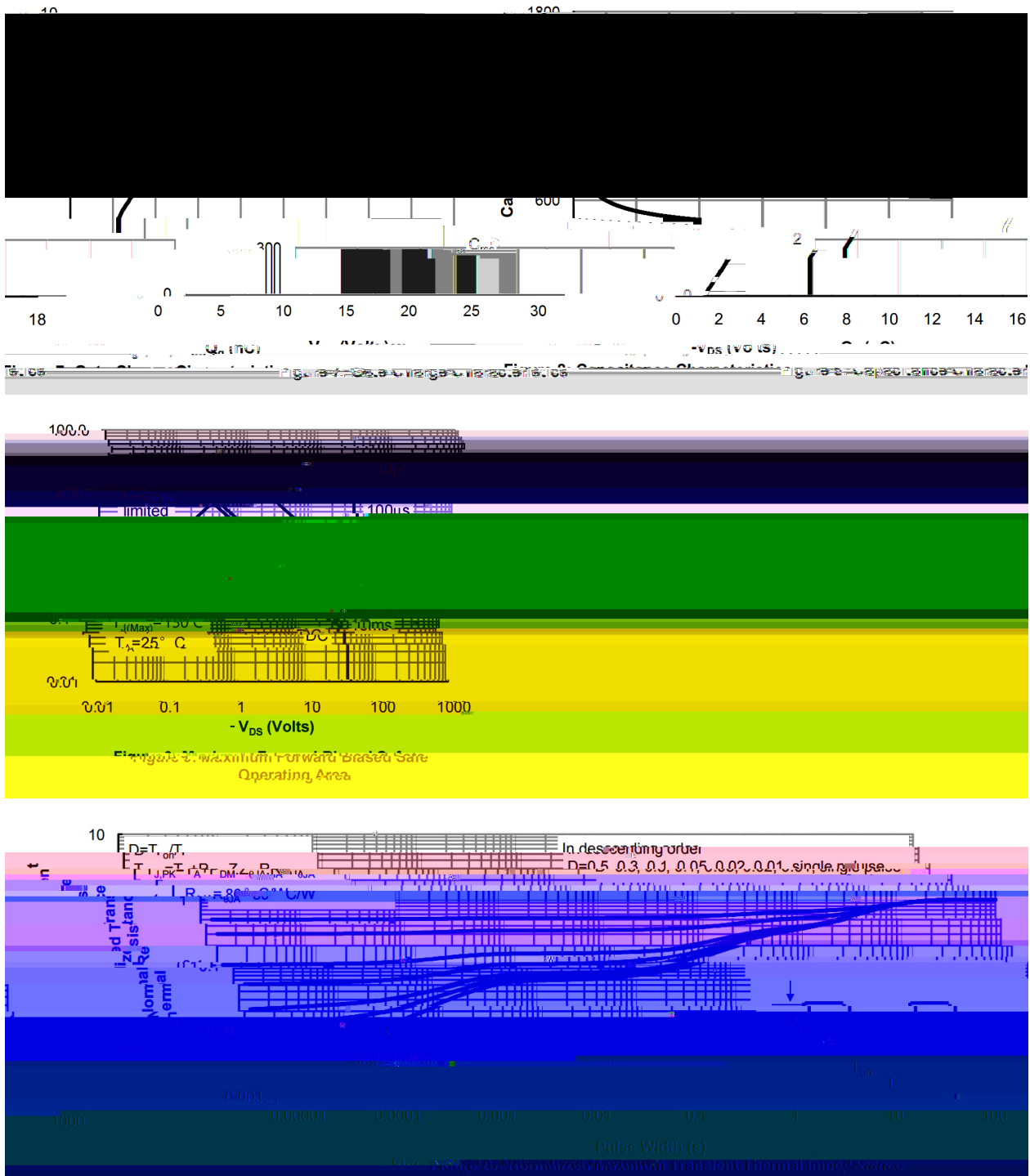
Static Drain-Source
On-Resistance

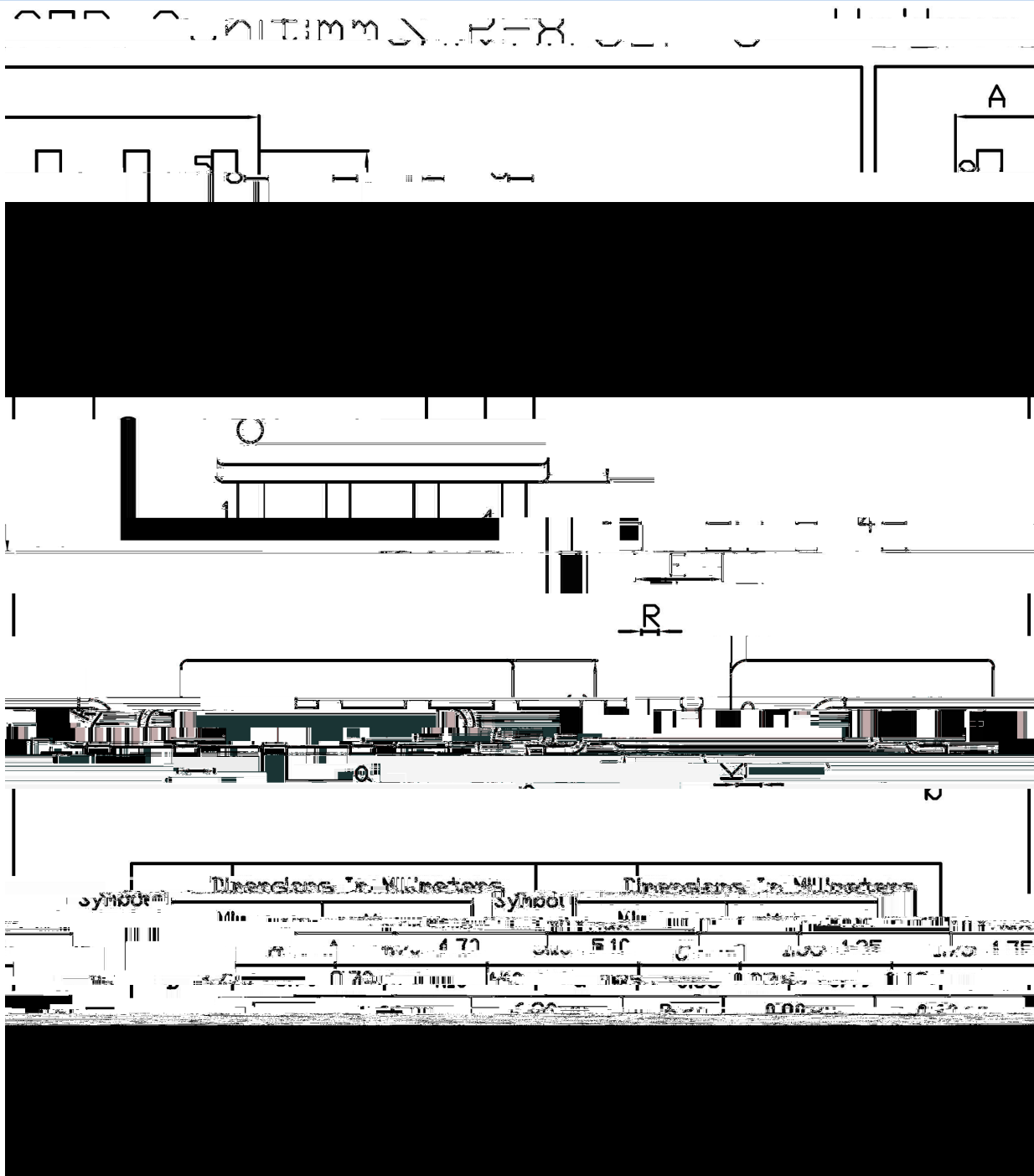
R_{10s} 58.7404 T_{m0} T_{c0} $T_{w(D)}$ T_{j0} 0.4958 498 r_{47998} 18.0 $T_{c433603}$ $T_{m371470}$ T_{c2} -20A $Therma.2192f5(33195)$ =0V

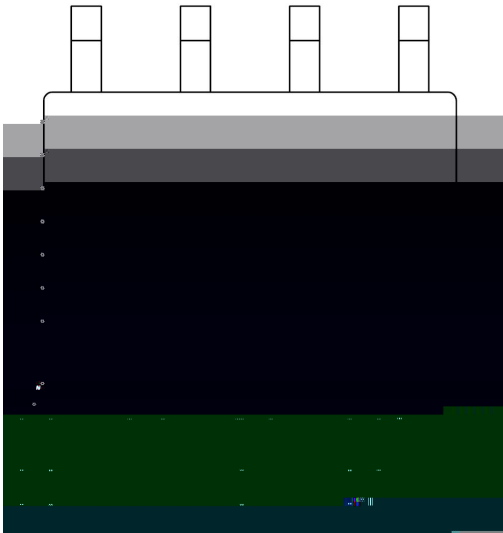
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Delay Time	t					



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Temperature Profile for IR Reflow Soldering(Pb-Free)

- 1

150 180

60 90sec;

1.Preheating:150~180 , Time:60~90sec.
- 2

245±5

5±0.5sec;

2.Peak Temp.:245±5 , Duration:5±0.5sec.
- 3

2 10 /sec.

3. Cooling Speed: 2~10 /sec.

260±5

10±1 sec.

Temp.:260±5

Time:10±1 sec

/ REEL

Package Type	Units	Dimension	(unit mm ³)
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