

# BRCM24C64SC

Rev.B Dec.-2018



DATA SHEET

BRCM24C64SC    SOP-8                      64 Kbit                      I<sup>2</sup>C

The BRCM24C64SC is 64Kbit I<sup>2</sup>C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. Halogen-free Product.

1.7V

2.5~5.5V

1Mhz

1.7~2.5V

**/ Pinning**

| Pin | Name | Type   | Description |
|-----|------|--------|-------------|
| 1   | E0   | Input  |             |
| 2   | E1   | Input  |             |
| 3   | E2   | Input  |             |
| 4   | GND  | Ground |             |
| 5   | SDA  | I/O    | /           |
| 6   | SCL  | Input  |             |
| 7   | WCB  | Input  |             |
| 8   | VCC  | Power  |             |

**/ Marking**

/ See Marking Instructions

**/ Absolute Maximum Ratings(Ta=25 )**

| Parameter                                 | Symbol           | Rating                     | Unit |
|-------------------------------------------|------------------|----------------------------|------|
| Storage Temperature                       | T <sub>stg</sub> | -65~+150                   |      |
| Operation Temperature                     | T <sub>opr</sub> | -40~+85                    |      |
| Maximum Operation Voltage                 | V <sub>cc</sub>  | 6.25                       | V    |
| Voltage on Any Pin with Respect to Ground | V <sub>pin</sub> | -1.0~ V <sub>cc</sub> +1.0 | V    |
| DC Output Current                         | I <sub>out</sub> | 5.0                        | mA   |
| Electro-Static discharge HBM mode         | ESD              | 6000                       | V    |

**/ Reliability Characteristic**

| Parameter      | Symbol | Test Conditions    | Min       | Typ | Max | Unit         |
|----------------|--------|--------------------|-----------|-----|-----|--------------|
| Endurance      | EDR    | 25℃ 3.3V Page mode | 1,000,000 |     |     | Write cycles |
| Data retention | DRET   |                    | 100       |     |     | Years        |



|           |        | 1.7V≤Vcc<2.5V | 2.5V≤Vcc≤5.5V |      |
|-----------|--------|---------------|---------------|------|
| Parameter | Symbol |               |               | Unit |

## / Functional Description

### H / Data Input

SDA SDA SCL ( 1 ) SCL  
( 1 )

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

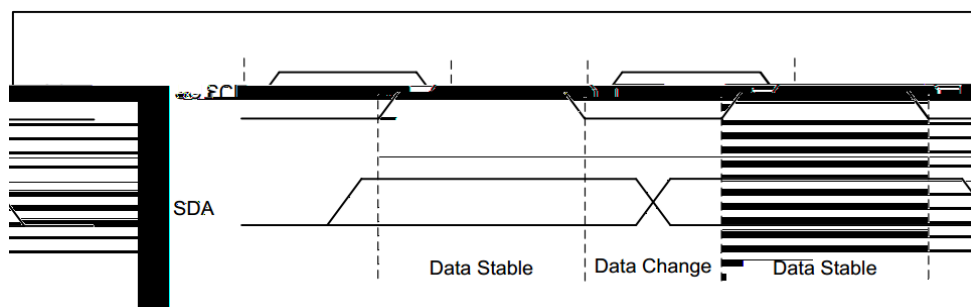


Figure 1 Data Validity

### H / Start Condition

SCL SDA  
2

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

### H / Stop Condition

SCL SDA

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A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C64SC in a standby power mode (see Figure 2).

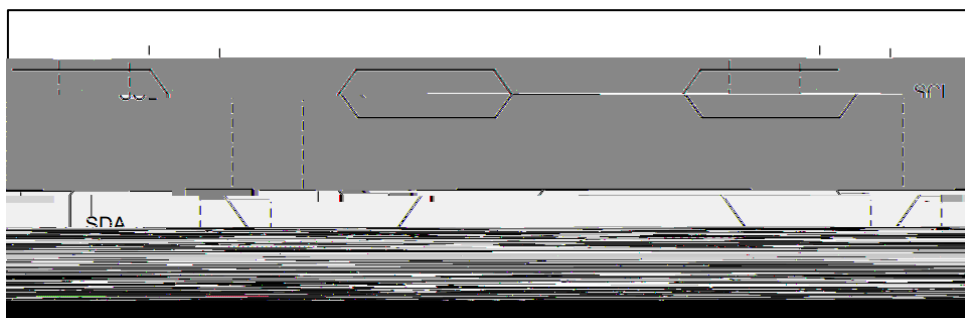


Figure 2 Start and Stop Definition

### H ACK / Acknowledge

ACK BRCM24C64SC BRCM24C64SC " 0 "  
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## / Functional Description

| Chip        | Access area   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| BRCM24C64SC | Normal Area   | 1     | 0     | 1     | 0     | E2    | E1    | E0    | R/W   |
|             | ID Page       | 1     | 0     | 1     | 1     | E2    | E1    | E0    | R/W   |
|             | Lock Bit      | 1     | 0     | 1     | 1     | E2    | E1    | E0    | R/W   |
|             | Serial Number | 1     | 0     | 1     | 1     | E2    | E1    | E0    | 1     |

Table 1 Device Address

| Chip        | Access area | Bit 7 | Bit 6    | Bit 5   | Bit 4    | Bit 3   | Bit 2     | Bit 1 | Bit 0 |
|-------------|-------------|-------|----------|---------|----------|---------|-----------|-------|-------|
| BRCM24C64SC | Normal A    | 1     | 12.e24T1 | 12.e601 | 1A121507 | 62-16(6 | -6(111507 | 62    |       |
|             |             |       |          |         |          |         |           |       |       |

/ Functional Description

A write operation requires one 8-bit data word address A12/A0 following the device address word and acknowledgment. Upon receipt of this address, the BRCM24C64SC will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the BRCM24C64SC will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the BRCM24C64SC enters an internally timed write cycle, all inputs are disabled during this write cycle and the BRCM24C64SC will not respond until the write is complete (see Figure 5).

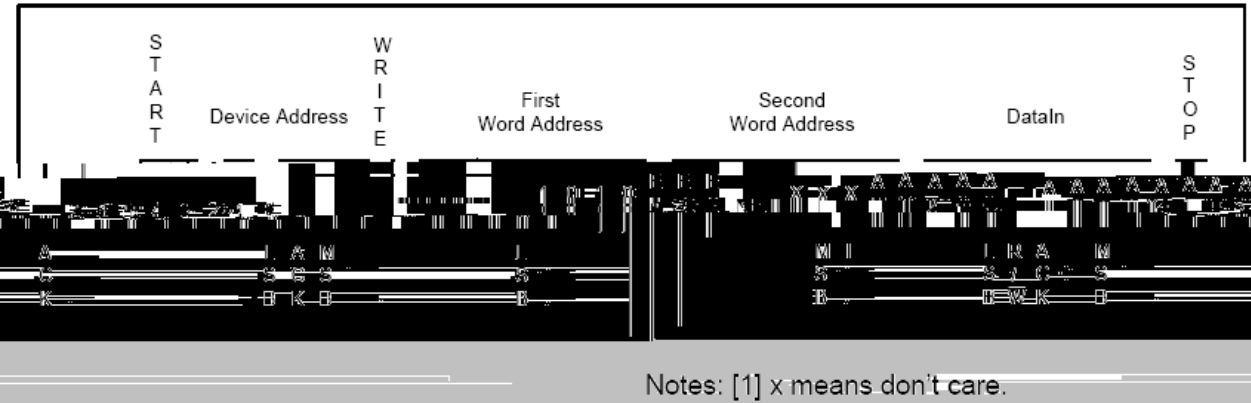


Figure 5 Byte Write

H / Page Write

BRCM24C64SC “ 0 ” BRCM24C64SC

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C64SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C64SC will respond with a “0” after

## **/ Functional Description**

The lower five bits of the data word address are

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## / Functional Description

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BRCM24C64SC, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BRCM24C64SC acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).

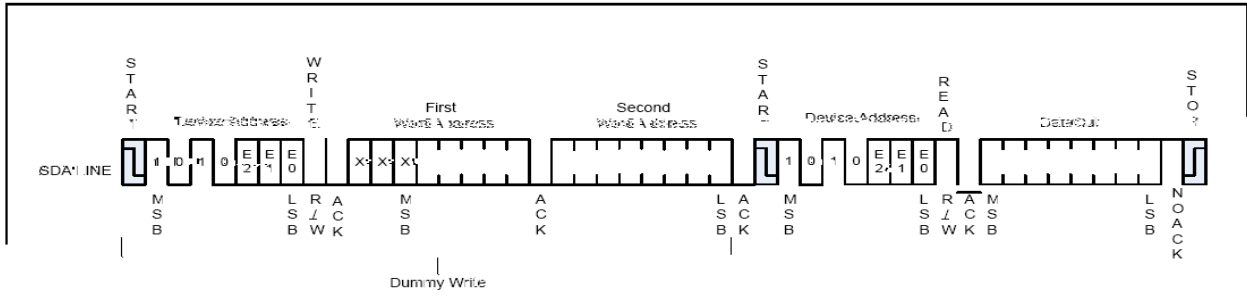


Figure 8 Random Address Read

## H / Sequential Read

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“ 0 ”

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Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C64SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

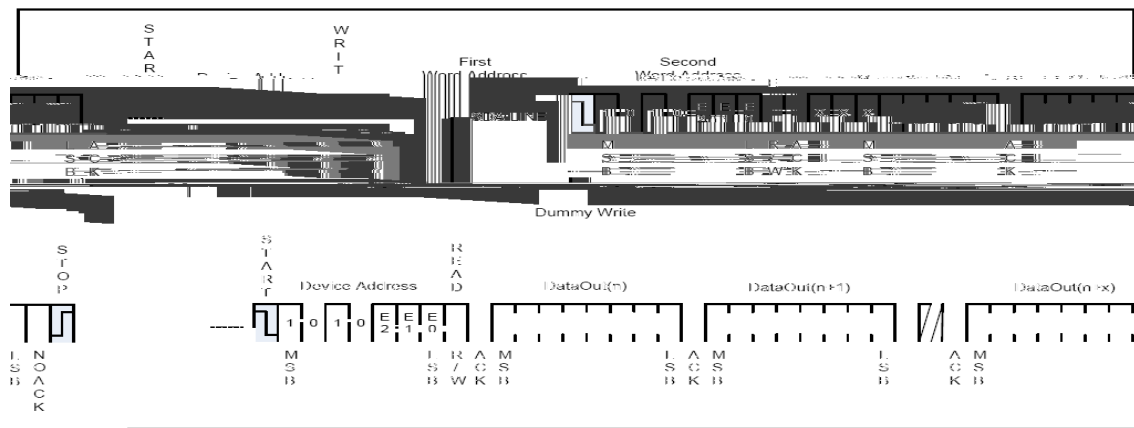


Figure 9 Sequential Read



## / Functional Description

|       |     |     |        |   |        |
|-------|-----|-----|--------|---|--------|
|       | A11 | A10 | " 10 " | 2 | " 10 " |
| 0800h |     |     |        |   |        |
| 128   | 16  |     |        |   |        |
|       | 128 |     |        |   | ACK    |
|       |     | 11  |        |   |        |

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 , a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a ' 10 ' sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 2 . If a word address other than ' 10 ' is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)

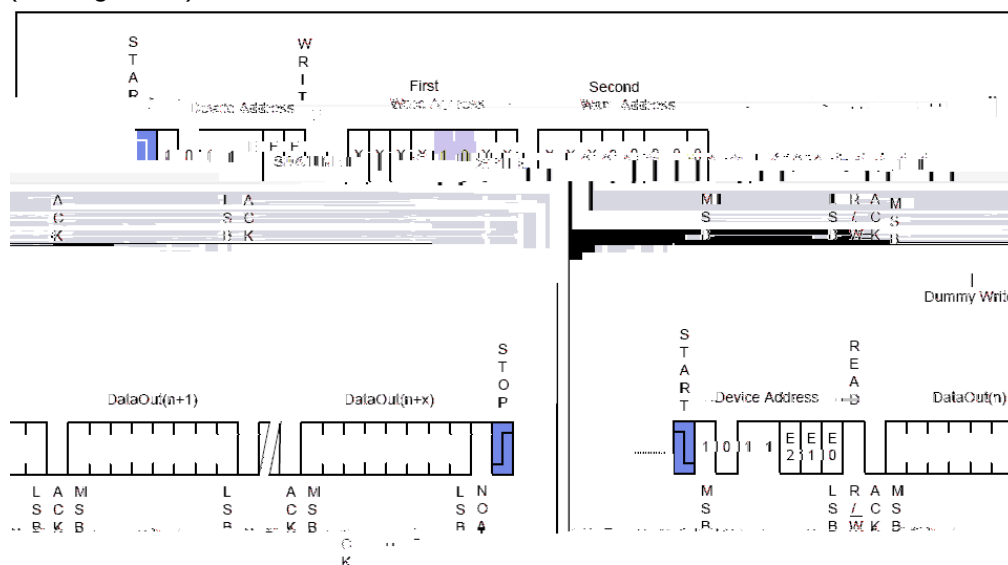
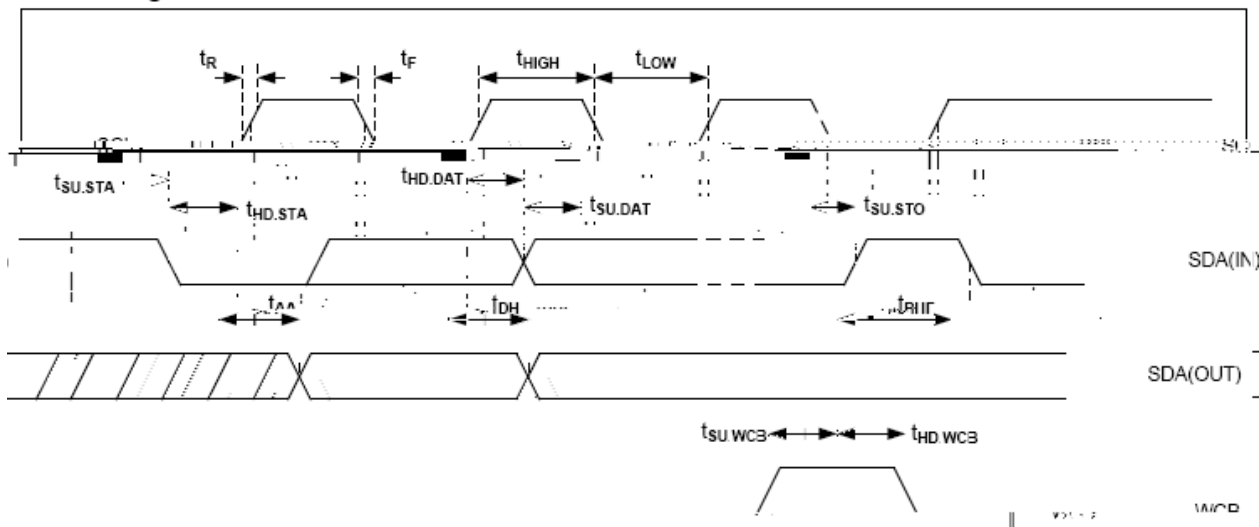


Figure 11 Sequential Read

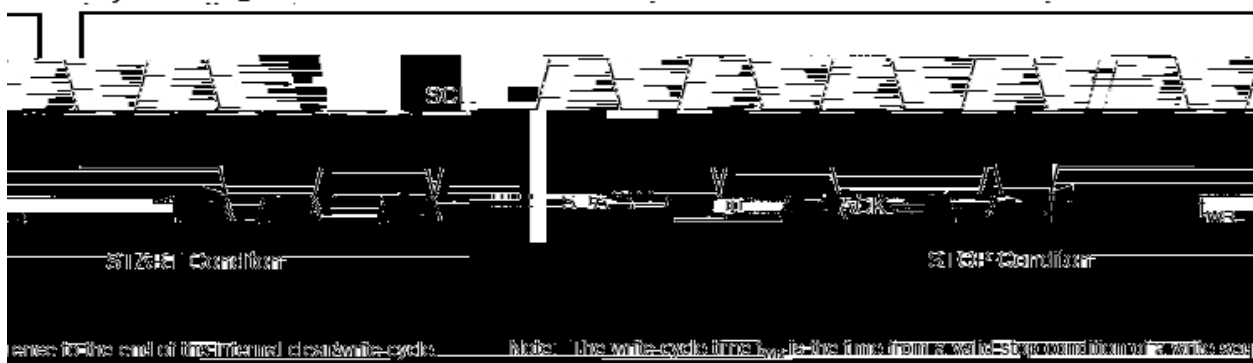


## / Time Sequence Diagram

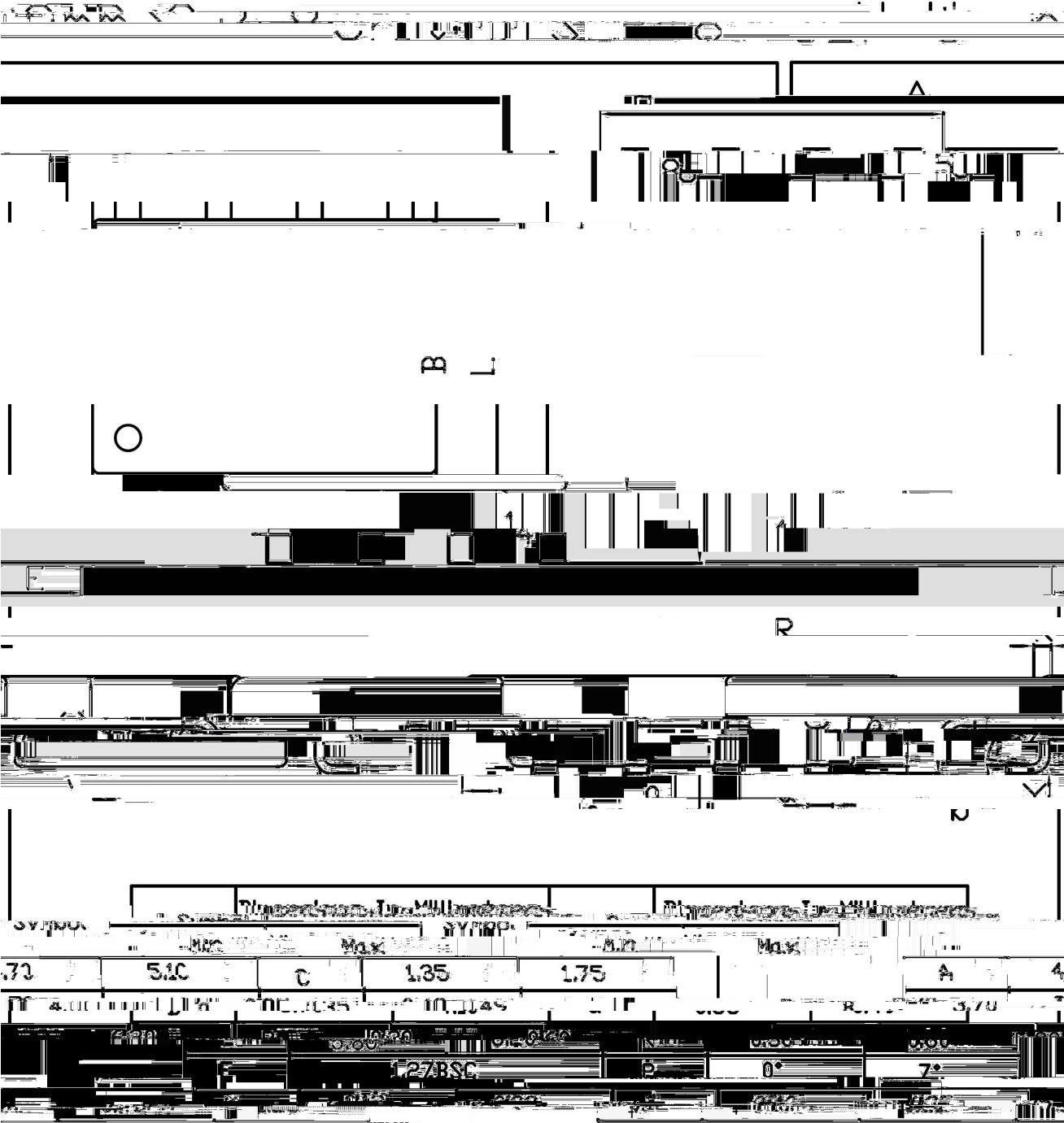
### Bus Timing



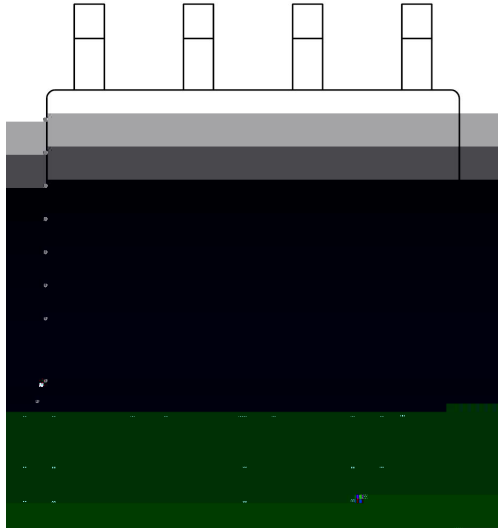
### Write Cycle Timing



/ Package Dimensions



**/ Marking Instructions**



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Note:

BR:                   Company Code.

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