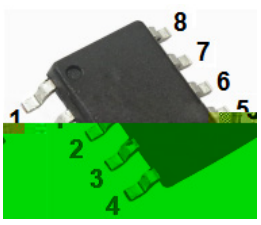
EUF P 57F35VF ĩ VRS0 ; Ṃ Ł ᴏʙᴊ ķ ᵢ̧ 5 Nelw ķ ⊥F ᴏʙᴊ ɥ Φ ɔ ˝Ḥ ڻ ح è ṇ
The BRCM24C02SC is 2Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. Halogen-free Product.

ɔ ◊ ɔ ψ
ѡ ṇ Ṫ ɔ Ⱨ₆ 41 : Y Ṫ ɔ ƥ 518~818Y ڑ ѡ ᶻ ˋH ت ļ ' 4 P k} Ṫ ɔ ƥ 41 : ~518Y ڑ
ѡ ᶻ ˋH ت ļ ' 733Nk} ψ
Ⱨ ı ă̈ F P RV ˋH ح ˝Ḥ ɔ ╚ 733xD ε ѡ ᶻ ζ ˝Ḥ ɔ ╚ 419 p D ε ѡ ᶻ ζ ψ
Ạ L̄ ≠ Ն ▾ └ ڑ Ꞓ ˝H ϕ ψ
˚ ẑ ₰ ح ≠ ề ψ
; È ` ˝ ₩ Ã ψ
è ⱪ ˚ ᴏʙᴊ ǐ ψ
ڜ ɾ ჳ ḧ ˝ 45 ; ɥ ẑ ˚ ᴺ ψ
₅ ḧ ˋH Ω ε ѡ ᶻ 8 p v ζ ψ
ↄ ˛ ó χ ح Ꝟ ˝Ω ᶻ 433 Ꝟ ˝Ω ˜Ω è ᶻ 433 ẇ HVG ε KE P ₩ Ã ζ ǐ̈ χ 9NY i ჳ ǐ̈
χ . 20533 p D›

Single Supply Voltage’
Minimum operating voltage down to 1.7V˝ 1 MHz clock from 2.5V to 5.5V˝ 400kHz clock from 1.7V to 2.5V’
Low power CMOS technology˝ Read current 400uA, maximum˝ Write current 1.6mA, maximum’
Schmitt Trigger, Filtered Inputs for Noise Suppression’
Sequential & Random Read Features’
8-byte Page Write Modes’
Write protect of the whole memory array’
Additional Write Lockable Page and 128-bit Serial Number’
Self-timed Write Cycle (5ms maximum)’
High Reliability’ Endurance: > 1 Million Write Cycles˝ Data Retention: > 100 Years˝ HBM: 6KV˝
Latch up Capability: +/-200mA;

Ķ ɾ ɔ ⅄ ʌ ᵢ̨ à Ã ʊ ѡ ɸ ᵗ ¨̈ ú ǐ̈ ɔ ´ ˝Y ɬ ɻ ჳ Ł ⅄

Household appliances, Network communications, Portable Bluetooth devices, Set-top boxes, Smart meters, Fingerprint unlocking devices



Slq	Qdph	W|sh	Ghvfulswlrq
4	H3	Lqsxw	ş ẋ ֆ ɹ
5	H4	Lqsxw	ş ẋ ֆ ɹ
6	H5	Lqsxw	ş ẋ ֆ ɹ
7	JQG	Jurxqg	֊ ɑ ş
8	VGD	L2R	Φ ̈Ω ̃Ω ڑ 2 ڑ
9	VF0	Lqsxw	Φ ̀H ت ڑ
:	ZFE	Lqsxw	í Ḥ ɔ Ẉ ΐ
;	YFF	Srzhu	ɔ ◊ ΰ

ð ٤ب ˝ / See Marking Instructions

̈Ω Parameter	٤ N Symbol	̈Ω Rating	Ꮋ Unit
Storage Temperature	T_{stg}	-65~+150	
Operation Temperature	T_{opr}	-40~+85	
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ ε Vcc+1.0 ζ	V
DC Output Current	I_{out}	5.0	mA
Electro-Static dischargeˆ HBM modeˇ	ESD	6000	V

̈Ω Parameter	٤ N Symbol	‗ :† Test Conditions	ѡ ṇ Min	Ɛ ʒ Typ	ѡ ᶻ Max	Ꮋ Unit
Endurance	EDR	25Ņˇ 3.3Vˇ Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

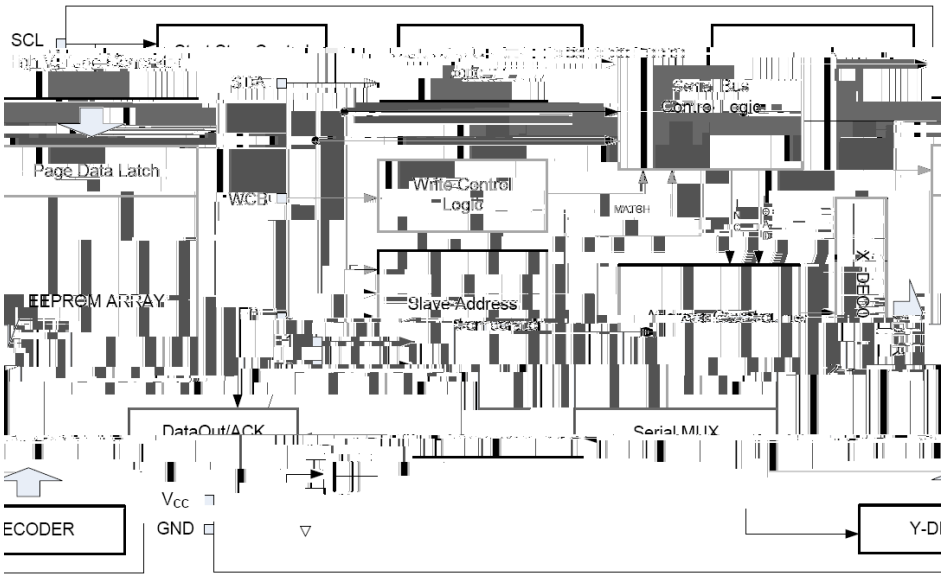
Parameter	Symbol

_ ° °

Ѝ Parameter	ㄱ N Symbol	1.7V≤Vcc<2.5V			2.5V≤Vcc≤5.5V			Ꮋ Unit
		ѡ ṇ Min	Ɛ ʒ Typ	ѡ ᶻ Max	ѡ ṇ Min	Ɛ ʒ Typ	ѡ ᶻ Max	
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	us
Data In Setup Time	$t_{SU.DAT}$	0.1	-	-	0.1	-	-	us
Inputs Rise Time[1]	t_R	-	-	0.3	-	-	0.3	us
Inputs Fall Time[1]	t_F	-	-	0.3	-	-	0.1	us
Stop Setup Time	$t_{SU.STO}$	0.6	-	-	0.25	-	-	us
Data Out Hold Time	t_{DH}	0.05	-	-	0.05	-	-	us
WCB pin Setup Time	$t_{SU.WCB}$	1.2	-	-	0.6	-	-	us
WCB pin Hold Time	$t_{HD.WCB}$	1.2	-	-	0.6	-	-	us
Write Cycle Time	t_{WR}	-	-	5	-	-	5	ms

Notes:AC measurement conditions:

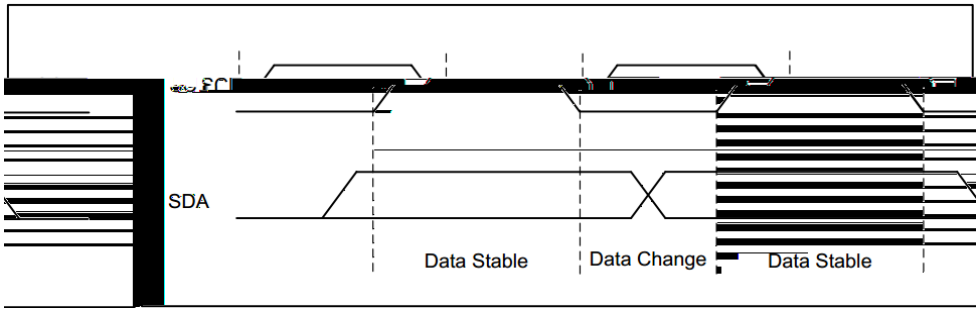
1. RL (connects to Vcc): 1.3k (2.5V, 5.5V), 10k (1.7V)
2. Input pulse voltages: 0.3 Vcc to 0.7 Vcc
3. Input rise and fall times: ≤50ns
4. Input and output timing reference voltages: 0.5Vcc



p

VGD Â ő ụ Ẃ ŕ ᵘ մ հ ֆ ᵗ ˜Ī ב VGD Â ő i ֏ ˜Ọ ˜Ō ő ĭ ƥ VF0 Ḥ ɔ Ẉ `H ˜ ˜ ώ + ḅ g, 4 ˝A˜ , VF0 ב ɔ Ẉ Ọ ֆ ֏ VGD ˝Ọ ˜Ō ώ Ṅ ı ∀ Ḋ ᴺ ǎ Ƀ ᴺ + ḅ g, 4 ˝A˜ , χ

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.



Ilj xuh 4 Gdwd Yd0lglw|

p

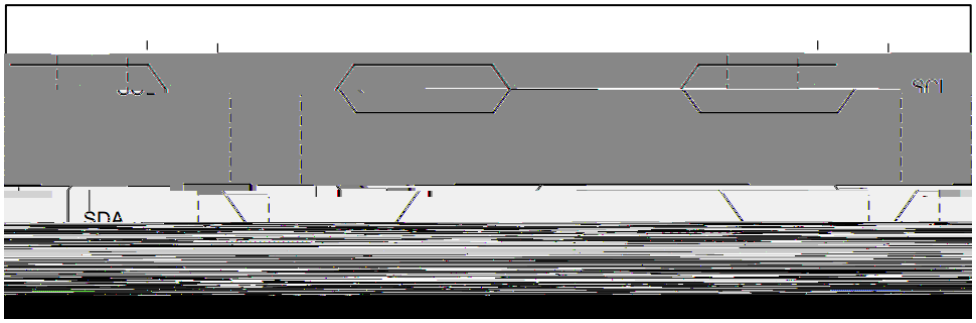
Ę VF0 ב ɔ Ẉ `H VGD ï ∪ ⌐ ε ב ɔ Ẉ ę Ḥ ɔ Ẉ ζ ∀ Ḋ ᴺ ∀ Ḋ ᴺ Ʊ ¨Ḥ ε ḅ g, 5 ˝A˜ ζ

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

p

Ę VF0 ב ɔ Ẉ `H VGD i ⌐ ε Ḥ ɔ Ẉ ę ב ɔ Ẉ ζ Ƀ ᴺ ς ẑ ˚ Ƀ ɲ ƀ EUF P 57F35VF ɹ ể ı ǎ ₩ Ã

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C02SC in a standby power mode (see Figure 2).



Ilj xuh 5 Vwduw dqg Vwrs Ghilqlwlrq

p

⅛ Ę ş χ ǎ ˝Ọ ˜Ō È ` ₡ Φ Ά Ã ڜ EUF P 57F35VF EUF P 57F35VF ڜ ɒ 3 ƀ ˊ ˜ ώ ف È ` Ẓ ∀ ε DFN ζ ı ƥ ∀ < `H ت Ω

All addresses and data words are serially transmitted to and from the SDA line on the rising edge of SCL. 24C02 can work in 400kHz clock frequency(t[0.236114 ...

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C02SC	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C02SC	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	0	0	A5	A4	A3	A2	A1	A0

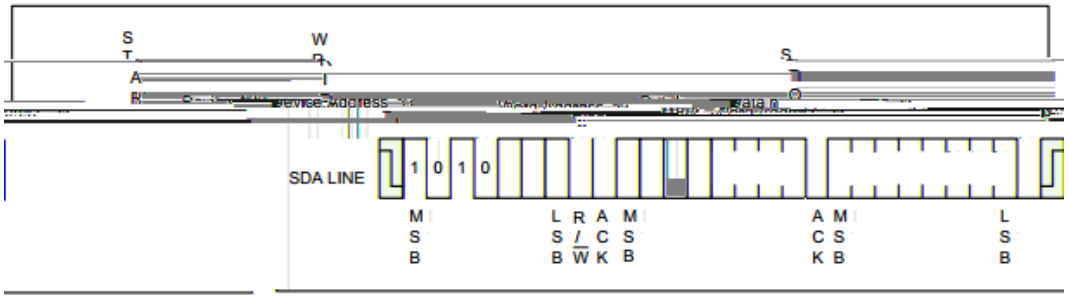


Figure 5 Byte Write

p

ˮ ˭ ˜Ḥ ЉÈ ` ˜Ḥ ˆ ĩ Ɑ ƥ ϒ Ƙ ˜Ḥ j ڳ ƁƗ ƥ. ɲ
EUF P 57F35VF ώ ϒ È ` ˝Ǫ˜Ω Ɑ Ɯ ʌ ʌ ڑ ˜ ^ ˝Ǫ˜Ω È EUF P 57F35VF ⅛ώ
˝Ǫ˜Ω È ` ʠu ɨ ɒ 3 ɓ Ƶ ϒ Ɑ Ɯ ڼ ص ɨ Ɓ ᴺ˥ ʌ Ɓ ˮ ˜Ḥ

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C02SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C02SC will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 6 Page Write

ƥ ì ώ ⅛ ˝Ǫ˜Ω È ˝Ǫ˜Ω È ş ẋ˝Ḥ 6 ɣ ƥ Ƞɲ ڼ ڍ ˝Ǫ˜Ω È ş ẋ ɣ j ɲ ϒ ɒ è ˮ
Φ ɣ ɻ Ẹ Ƞɨ ă È ş ẋ ڑ ˮ ڑ ϱ `H ˭ È ` ώ ƥ ˮ Ã˘ ḅ ' ڳ
EUF P 57F35VF ˝Ǫ˜Ω È ʌ ص ; ¨ ˝Ǫ˜Ω È ş ẋ Ṅ˘ ڃ ˝Ǫ˜Ω Ṅ qḥu ˝ ˮ ˜Ḥ Ω ڑ ş
ẋ˘ ڃ ĩ Ẹ ˮ ˭ ώ È ` ˮ ˭ ϒ È `

The lower three bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 8 data words are transmitted to the BRCM24C02SC, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

p

ñ ሀ ሐ H Ω Â Ḋ Ẋ ŕ EUF P 57F35VF ڑ ő Ꝍ Ẓ ٧ ڎ Ĩ ف ں گ ٧ Ḋ ᴺ ̊ ƥ Ф ᵻ ş ϰ È ` ˭ ς 2 ყ Ђ ´ ″A ⍽ ″Ḥ ω ƥ ሀ Ω Ḣ ă EUF P 57F35VF ė Ẓ ɒ 3 ɓ ƥ ς ỗ ẑ ˚ ٨ ٨

Once the internally timed write cycle has started and the BRCM24C02SC inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the BRCM24C02SC respond with a “0”, allowing the read or write sequence to continue.

p

‰ ᾽ ˜ ε 49 È ` ζ ĩ ڜ ŕ ˜ ˭ Ꝍ ƥ ς ₩ Ã ï Ẋ ⇔ ɔ ḧ Ę ᵻ ‰ ᾽ ˜ ˭ ″Yᴨ Ĭ ″Yᴨ ŕ ль ˜ ε è Ƹ ˚ ζ ʊ ѽ ⍽ ɲ ǂ Ã ω Ꝍ ï χ

+d, Ф ᵻ ٨ ʒ ‰ ᾽ χ 4344e ψ

+e, ş ϰ ყ D8 2 D7 Ỵ 3 ỗ 4 ٨ ş ϰ ყ D : 2 D9 ọ ɛ ɒ 33 ɓ ψ

+f, ş ϰ ყ D6 2 D3 ḧ Θ ‰ ᾽ ˜ ˭ ⍽ È ` ş ϰ ḅ ᾽ ‰ ᾽ ˜ ˭ ĩ ɔ ḧ ⍽ ƥ ‰ ᾽ ˜ ˭ ″Yᴨ Ω ڑ ڑ ⍽ ″Ω Ẑ Ω È ` j ɑ Ẓ ٧ ε Q r DFN ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

(a)Device type identifier = 1011b.

(b)Address bits A5/A4 are don’t care while address bit A7/A6 which must be ‘00’.

(c)Address bits A3/A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

p

ɔ ḧ ‰ ᾽ ˜ ˭ ″Yᴨ ε ɔ ḧ ᒪG ζ ⇔ ɔ ḧ ‰ ᾽ ˜ ˭ ƥ ς ₩ Ã ï ڦ Φ O r fn ᒪG ″Yᴨ ٨ È ` ε è Ƹ ˚ ζ ʊ ǂ ḅ ï χ

+d, Ф ᵻ ٨ ʒ ‰ ᾽ χ 4344e ›

+e, ş ϰ ყ D9 4 Ʊ ყ Ỵ ›

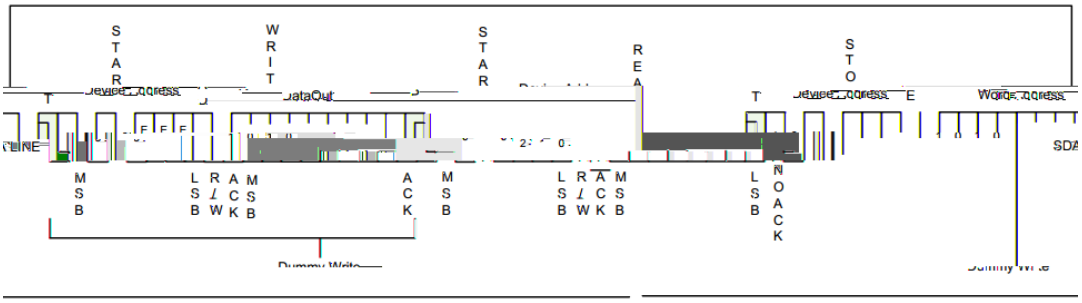
+f, Ω Ẑ Ω È ` ọ ɛ ٧ ڦ {{{{ {{4{ Ʊ { Ỵ 3 ỗ 4

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

(a)Device type identifier = 1011b.

(b)Address bit A6 must be ‘1’ all other address bits are don’t care.

(c)The data byte must be equal to the binary value xxxx xx1x, where x is don’t care.



Ilj xuh ; Udqg r p Dgguhvv Uhdg

p

p

‰ ˝ ε 49 È ` ζ ĩ ڑ ɾ ˝ ˭ Ɋ ɒ ς ₩ Ã ï Ẋ ⇔ ẹ ḧ ˝ ˭ Ɋ ɳ ص ς ˝ ˭ ″Yɒ ς Ỉ ″Yɒ ɾ ɔ ς ɒ ε ˡ ₅ è Ƨ ˚ ζ ῶ ՛ ɲ † Ã Ф ᵻ ɻ ȝ ‰ ˝ ɻ ḧ Θ 4344e ş χ ɥ D : 2 D9 ọ ɛ 3 ắ D8 Ỵ ş χ ɥ D7 2 D3 ḧ Θ ‰ ˝ ՛ È ` ş χ ŁG ˝ ˭ ŀ ς ՛ È ` ″Ɋ j ệ ʌ ص ˝ ˭ ɀ ɳ ε ḅ ɥ ɻ 43g ς ‰ ˝ ˋH È ` ″Ɋ Ẓ ṇ ắ ɻ 9 ɨ ŁG ˝ ɀ ɳ 49 È ` ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same prot7pol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A7/A6 must be 0 while A5 is don't care, and the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 6, as the ID page boundary is 16 bytes).

p

Ɋ ɳ ص Ф ᵻ ڑ ≠ ḧ Ȧ Ă ɒ [‰ ˝ ″Yɒ . ″Ɋ ″Ω È `]ʃ ₅ ¶ ‰ ˝ ˭ ẹ ḧ 2 ɻ ẹ ↑ õ ḅ ' ˝ ˭ ˭ ' ẹ ḧ ¨ Ф ᵻ ف ɨ DFN ḅ ' ˝ ˭ ˭ ɋ ẹ ḧ ¨ Ф ᵻ ف ɨ Q r DFN/+ ḅ ɡ 43 ″Ã˜ ,

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked (see Figure 10).

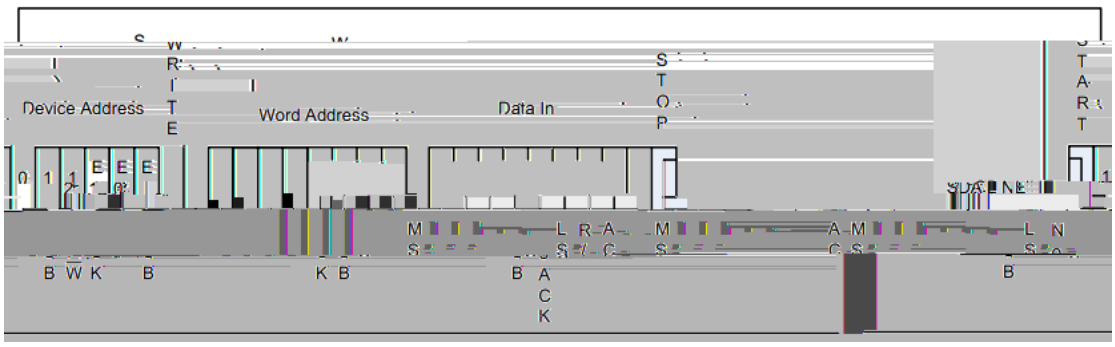


Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

p

‰ ˝ ε 49 È ` ζ ĩ ڑ ɾ ˝ ˭ Ɋ ɒ ς ₩ Ã ï Ẋ ⇔ ẹ ḧ ς ẑ ˚ ᴺ ɻ ˚ ̲ ẑ ς ẑ ˚ ɹ ŀ ɾ ´ 4 ″Ã˜ ş χ Ն ″Ο Ɋ ɾ ≠ ḧ È ` ş χ ọ ɛ ẑ ˚ ᴺ ę ∨ Ḋ ş χ ς ″Ω 45 ; ɥ Ɋ - ɻ ᴺ ˡ ş χ ″Y ɟ ɒ Ẃ h HHSUR P Ƨ ˚ ẑ ˚ ᴺ ę ɹ ɨ % Ẓ ″Ε Φ ɒ ɓ ẑ ˚ ς ắ ˚ ̲ ẑ ς ɲ ɻ մ Ɋ ɹ ş χ ″Y ɟ Ф ɻ ɟ ḅ ' ″Ḥ ĩ HHSUR P Ƨ ˚ ẑ ˚ ᴺ ę ĩ ″Ḥ ′Y Ẹ ş χ ς ş χ ″Y ɟ Ṅ ɒ Ɯ ɜ ɻ ɥ ɻ i ɯ ɾ 4 ẑ ˚ ᴺ ę ɻ ş χ Ɋ ᵘ ɥ ɻ ς ẑ ˚ ᴺ Ṁ ɨ ẑ ˚ ᴺ j

℅ ᵘ ẑ˚ ᴺ▯È ş ϰ D: D9 ʁ ẑ˚ ɒ 43 ɓ ḅ ´ 5 ¨A˜ ▯Ĺ Ф ş ϰ ḅ ' ɾ ɒ 43 ɓ Ɋ ᵘ▯ È ş ϰ ɑ ψ Ф ᵻ Ṅ ɟ ' ḧ Θ▯Ɋ Ω ε˜ χ ḅ ' Ẓ ɾ ϒ ẑ Ű Ὼ ƈ ẑ˚ ᴺ▯ Ч È ` „ È ş ϰ ɟ ₓ ɭ ;3k ζ

Ẹ ј 45; ʁ ε 49 È ` Ɋ Ω ζ ẑ˚ ᴺ▯ Ṕ Ή Ⲗ Ⲗ ƈ ¨E ī è Ṅ Ṁ ي ʉ▯ẑ˚ ᴺ Ɋ Ω ƈ Ɋ Ὲ ş ϰ Ṅ˘ ƈ ɬ 45; ▯Â˘ ʁ ẑ˚ ᴺ È ş ϰ Ẹ ỉ í ≡ ω Ẓ ¸ ε DFN ζ Ή ẑ˚ ᴺ ƈ ¨Ḥ Ⲗ Ƀ Ẋ Ƀ ε ð g, : ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

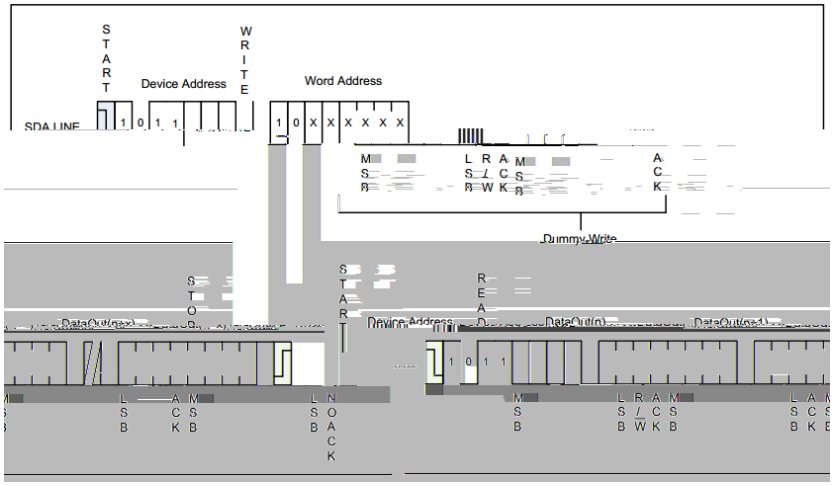
Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 on page 9, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a ‘10’ sequence in bit A7 and A6 of the word address, regardless of the intended address as depicted in Table 2 . If a word address other than ’10’ is used, then the device will output undefined data.

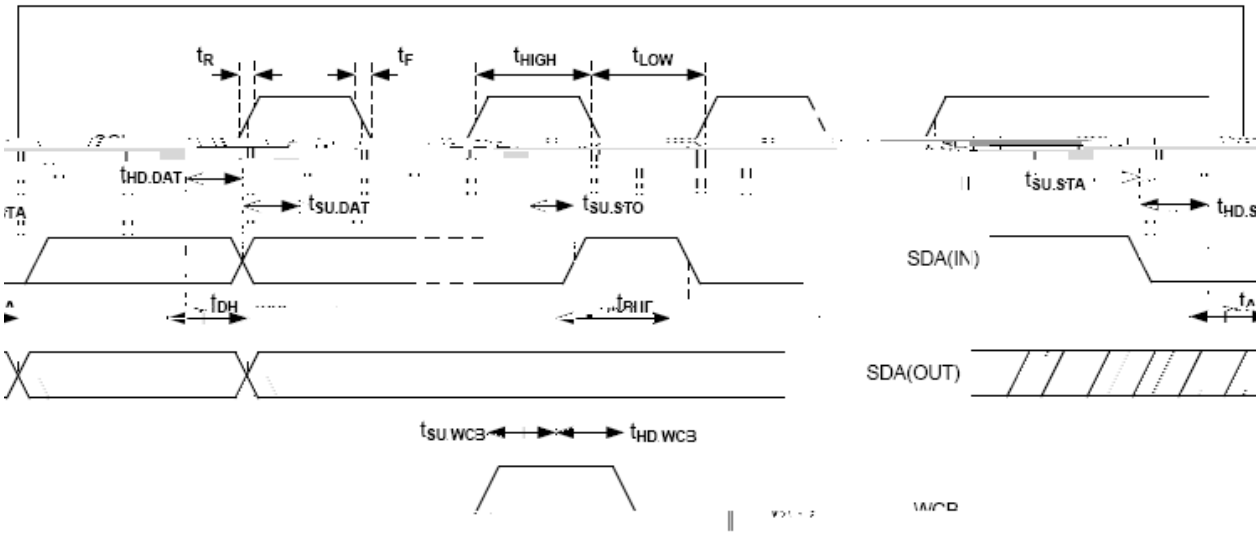
Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)

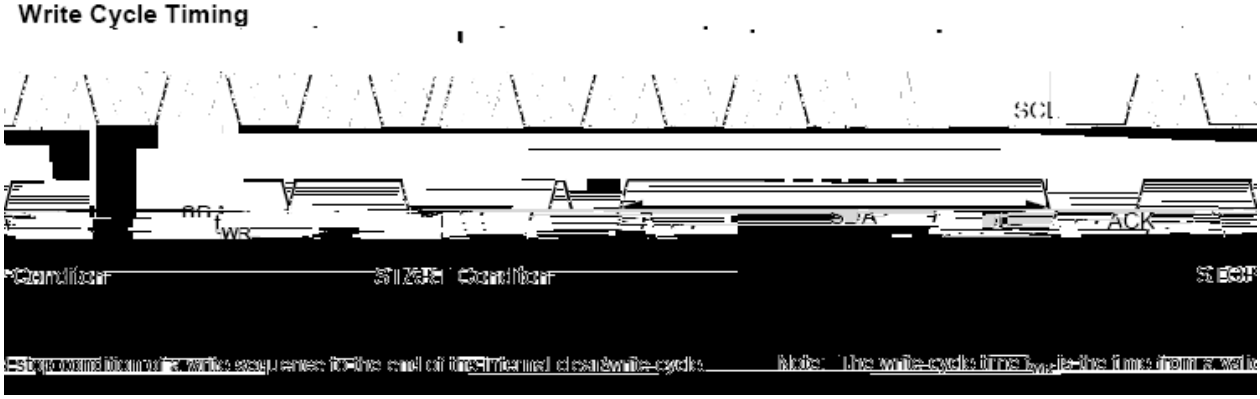


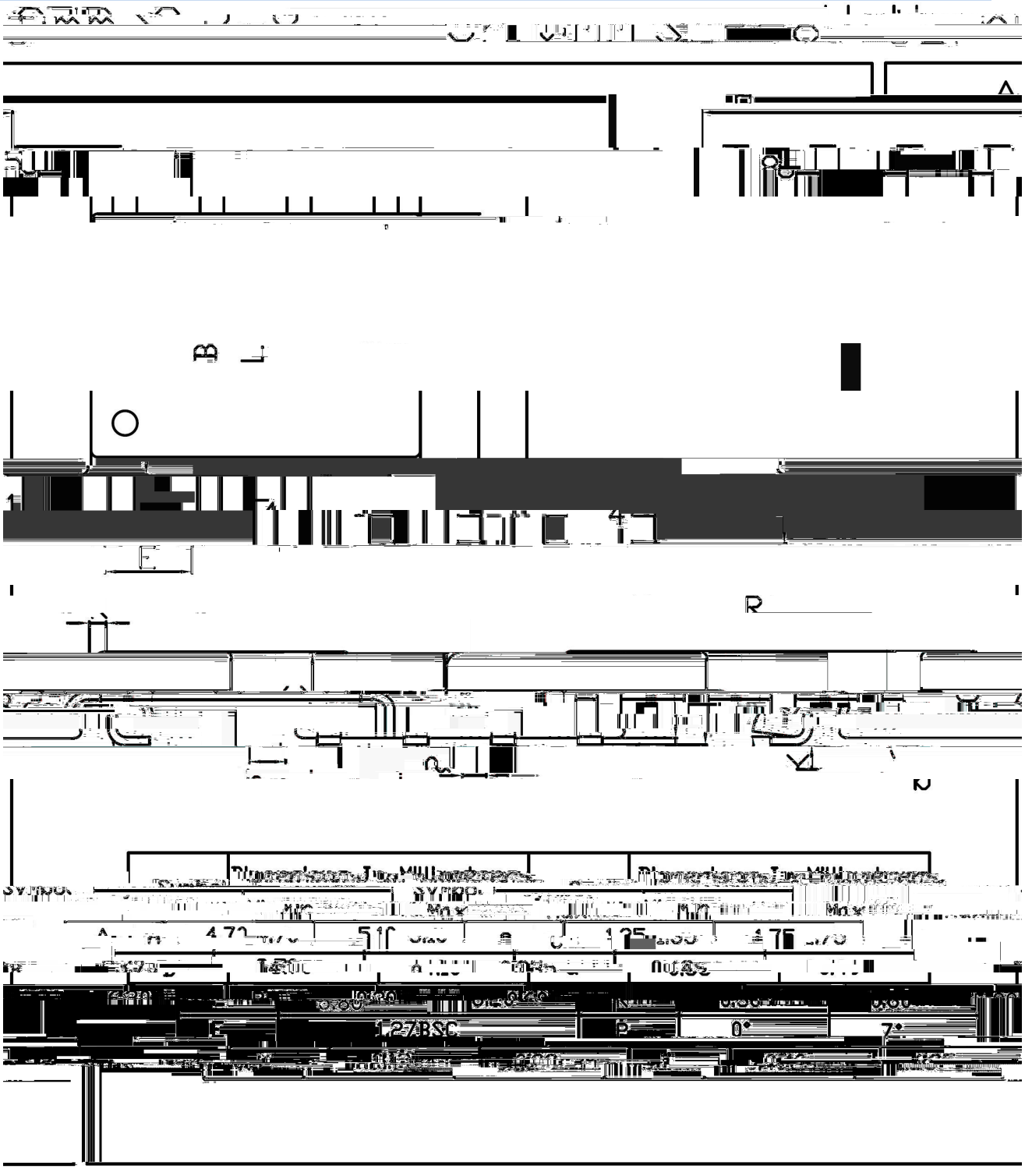
Ilj xuh 44 Vht xhqwld Uhdg

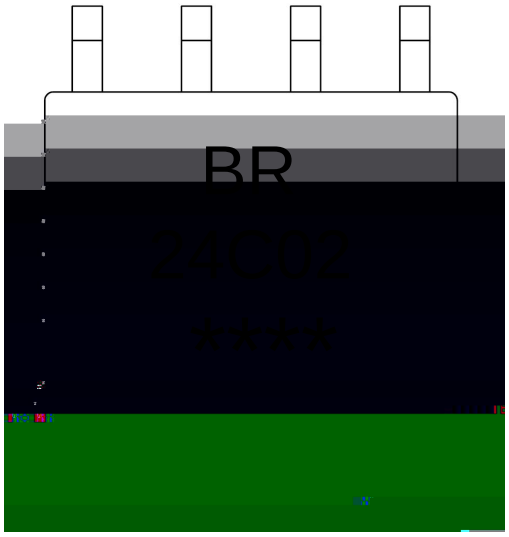
Bus Timing



Write Cycle Timing



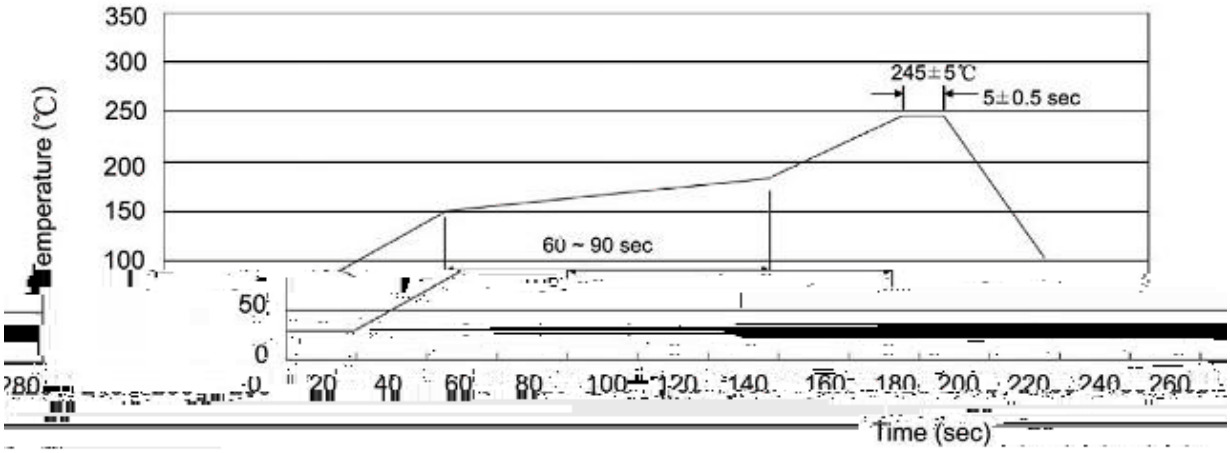




Note:

BR:	Company Code.
24C02:	Product Type.
****:	Lot No. Code, code change with Lot No.

Temperature Profile for IR Reflow Soldering(Pb-Free)



ب ″ χ

1 Ĺ ♬ □ ỷ 150 180 `H ڑ 60 90sec;

2 Š □ ỷ 245 ° 5 `H ڑ `Y ٨ 5 ° 0.5sec;

3 ì ٧ ↄ ھ ỷ 2 10 /sec.

Note:

1.Preheating:150~180 , Time:60~90sec.

2.Peak Temp.:245 ° 5 , Duration:5 ° 0.5sec.

3. Cooling Speed: 2~10 /sec.

`Y

□ ỷ χ 260 ° 5 `H ڑ χ 10 ° 1 sec

Temp.:260 ° 5 Time:10 ° 1 sec

` Ь / REEL

Package Type	Units					Dimension		(unit mm³)
	Units/Reel /	Reels/Inner Box /	Units/Inner Box /	Inner Boxes/Outer Box /	Units/Outer Box /	Reel	Inner Box	Outer Box
SOP/ESOP-8	4,000	2	8,000	6	48,000	13 ρ ×12	360×360×50	380×335×366×12